DETAILED ACTION

1. Receipt is acknowledged of amendments/arguments filed on 2/19/2008.

2. Claims 34-46 are presented for examination.

3. This application is a 371 of PCT/EP04/53548 filed on 12/16/2004.

Priority

4. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

6. Claims 34-46 are rejected under 35 U.S.C. 102(e) as being anticipated by Ookawa et al. (U.S. 6,585,166).

Re claims 34 and 40: Ookawa et al. {hereinafter referred as "Ookawa"} discloses composite IC card, which includes a processor block {through the gate circuits 7 and 9} and at least two communication interfaces {herein a contact coupling through the voltage detector 19 and a non-contact coupling through the voltage detector 18} with and/or without contact, at least one of the communication interfaces being able to provide the portable object with electric power {herein DC voltage} (col.2, lines 61-67), the process comprising the following steps a state of availability of at least one electric power resource on one of the interfaces and selecting at least one of the electric power resources (col.3, lines 9-67; col.4, lines 167), generating and providing an interrupt signal {through the logic gate circuit 15} to the processor block on a variation in availability of at least one of the electric power resources, and processing the interrupt signal in the processor in order to allow selection of the electric power resources (col.5, lines 25-57).

Re claim 35: Ookawa teaches an apparatus, wherein an interrupt signal is generated by a resource controller {herein interpreted as the clock detectors 13 & 14, as shown in fig.# 4} according to the transitions of statuses of availability of at least one electric power resource (col.4, lines 34-67; col.5, lines 1-42).

Re claim 36: Ookawa discloses an apparatus, wherein the interrupt signal is generated for the following transitions: transition from a state of low power supply via the contact interface to a state of power supply via the contactless interface, the voltage available via said contactless the interface being greater than a threshold voltage; transition from a state of supply via the contactless interface to a status of cessation of this supply, the voltage received by the contactless interface being lower than a threshold voltage; transition from a state of supply via the contactless interface to a state of supply

via the contact interface; transition or reset sequence commanded by the contact interface, with supply via the contact interface (col.3, lines 5-57).

Re claims 37 and 44: Ookawa teaches an apparatus, wherein the process comprises at least one step of immediate warning for fully simultaneous management of power and/or clock resources (col.6, lines 5-13).

Re claims 38 and 45: Ookawa teaches an apparatus, wherein the immediate warning step causes a diversion phase {herein the logic circuit 15} of the electric power resources in order for the electric power to be supplied at least in part via the contactless interface (see figs.# 4, 6-7; col.5, lines 25-57).

Re claim 41: Ookawa discloses an apparatus, further comprising means of immunity including a diode 11 for limitation of power consumption from the contactless interface; and a logical gate switching between two modes of power supply via the contact interface or via the contactless interface (see figs.# 1, 3-4, 6-7; col.4, lines 4-10).

Re claim 39: Ookawa teaches an apparatus, wherein the portable object comprises a chip 20 and wherein the process includes at least one logical phase forming a sleep controller so that the chip complies with constraints of lower power consumption during sleep states (col.3, lines 35-39).

Re claims 42 and 46: Ookawa teaches an apparatus, wherein the means of immunity comprises at least one wired mechanism that detects the presence of a power supply resource derived from the contact interface and derived from the contactless interface; this said mechanism possessing at least two registers {herein gate circuits 7 & 9} via which the means of immunity indicate the status of the supply resources (col.3, lines 8-65); wherein any modification in these registers results in an alert signal {herein

logic circuit 15 inputs output signal from the clock detectors 13 & 14}, in the form of interruption; and wiring connecting the mechanism to a processing block, so that the means of immunity, after reading contents of the registers selects the power source to be used (col.5, lines 25-57).

Re claim 43: Ookawa discloses an apparatus, wherein the device comprises a chip and wherein the means of immunity comprises a wired mechanism provided in the chip so that the selected source supplies the chip with electricity (col.3, lines 35-39).

Response to Arguments

7. Applicant's arguments with respect to claims 34-46 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Arisawa (U.S. 6,560,082) teaches power source unit and card-like memory medium.

Shigemasa et al. (U.S. 6,737,884) teaches power-on reset circuit and IC card.

Nishizawa et al. (U.S. 7,325,746) teaches memory card and semiconductor device.

Sue et al. (US 2004/0027110) teaches power supply control apparatus.

Lee (US 2005/0274803) teaches portable dual-mode contact and contactless communication device.

Fruhauf (US 2005/0045720) teaches method and apparatus for a USB and contactless smart card device.

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to EDWYN LABAZE whose telephone number is (571)272-2395. The examiner can normally be reached on 7:30 AM - 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steve Paik can be reached on (571) 272-2404. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/EDWYN LABAZE/
Primary Examiner, Art Unit 2887
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